PHOTOMASK AND METHOD FOR EXPOSING CHIP PATTERN

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

The invention relates to a photomask for exposing a chip pattern onto a wafer and a method for exposing a chip pattern.

This application is a counterpart of Japanese patent application, Serial Number 304002/2002, filed October 18, 2002, the subject matter of which is incorporated herein by reference.

DESCRIPTION OF THE RELATED ART

Before mass-producing chips, a prototype of a chip is always fabricated and the prototype of the chip has to be evaluated. In order to manufacture of the prototype of the chip, a reticle mask (one type of a photomask) on which a chip pattern corresponding to prototype of the chip is formed has to be fabricated.

For a reticle mask for prototype use, a reticle mask 100 on which only the same types of chip patterns A are formed, as shown in Fig. 15(A), and a reticle mask (multichip mask) 102 on which multiple types of chip patterns A, B, C are formed at the same ratio, and the like, as shown in Fig. 15(B), have been conventionally used.

There is an advantage that the reticle mask 100 for prototype use can be used for mass-production as it is if there is no problem. However, if any problem arises in the chip patterns A, it is necessary to design and

fabricate again a reticle mask for forming a chip pattern for prototype use in place of the chip patterns A, and hence it takes time to make the transition to the mass-production. Further, for the multichip mask 102, it is necessary to design and fabricate again a mask for mass-production so as to utilize the exposure area of the projection exposure apparatus (the apparatus is ccalled as an aligner or a stepper.) for mass-production to the greatest extent, and hence there arises a problem of increase of cost.

Further, as shown in Fig. 16, there is proposed a method of exposing only an intended chip of a multichip mask 104 on which multiple (four types in Fig. 16) different patterns are formed onto a wafer 108 using a projection lens 106, for example, as disclosed in Japanese Laid-Open Patent No. 11-305418, and also there is proposed a method of exposing only an intended chip on a wafer while shielding an exposure area other than the intended chip, for example, as disclosed in Japanese Laid-Open Patent No. 06- 020911.

However, these method have a problem that it takes much time for processing chips because the exposure area is not utilized to the greatest extent.

SUMMARY OF THE INVENTION

The present invention has been developed in view of the foregoing problem of the prior art, and it is an object of the present invention to fabricate prototype and mass-produce chips by the same photomask and the exposing area of the projection exposure apparatus can be utilized to the greatest extent.

The photomask in one aspect of the present invention is that a first

mask pattern which has first chip patterns and which has a first size corresponding to a maximum exposure area of a projection exposure apparatus; and a second mask pattern which has second chip patterns different from the first chip patterns, which has a second size smaller than the first size, and which is arranged adjacently to the first mask pattern.

According to the photomask of the aspect of the present invention, multiple same first chip patterns are formed on the first mask pattern serving as the maximum exposure area of the projection exposure apparatus, and the second chip patterns which are different from the first chip patterns are formed on a second mask pattern provided adjacently to the first mask pattern.

Accordingly, it is possible to expose the first and second chip patterns on the wafer at a time, and the evaluation thereof can be made at the same time. Further, since the maximum exposure area of the projection exposure apparatus can be subjected to exposure in the case of exposing only the same first chip patterns, the time for processing the wafer can be shortened without wasting exposure area.

The photomask in another aspect of the present invention is characterized to be a mask for mass-production.

According to the photomask of the aspect of the present invention, it is not necessary to redesign and re-fabricate a photomask for mass-production if the first chip patterns are evaluated when the chips are prototyped and the first chip patterns satisfy the specification of mass-production, and hence the term for developing chips can be reduced and the fabricating cost of the photomask can be reduced.

The photomask according to still another aspect of the present invention is characterized in that it is the photomask according to abovementioned aspect of the invention and the first mask pattern is provided at the center and the second mask pattern is provided at the periphery of the first mask pattern.

According to the photomask of the aspect of the present invention, first mask pattern is provided at the center and the second mask pattern is provided at the periphery of the first mask pattern. For example, in the case where an area of the second mask pattern is equal to that of the first mask pattern, if the second mask pattern is concentrically provided on one area which is adjacent to the first mask pattern, it becomes an oblong mask, thereby producing a wasteful area at the upper and lower portions thereof. However, if the second mask pattern is provided at the periphery of the first mask pattern while dispersing it, an area of the photomask can be utilized efficiently, thereby not producing a wasteful area. Accordingly, a fabricating cost of the photomask per piece is reduced.

According to still another aspect of the present invention, there is provided a method for exposing chip patterns on a wafer, the method includes providing a photomask which includes a first mask pattern and a second mask pattern, the first mask pattern having first chip patterns and arranged in an area corresponding to a maximum exposure area of a projection exposure apparatus, and the second mask pattern having second chip patterns different from the first chip patterns and arranged adjacently to the first mask pattern. The method also includes aligning the maximum exposure area of the projection exposure apparatus with a part of the first

mask pattern and a part of the second mask pattern, and exposing a part of the first chip patterns and a part of the second chip patterns on a first wafer. The method also includes aligning the maximum exposure area of the projection exposure apparatus with the first mask pattern and exposing the first chip patterns on a second wafer.

According to the method of the aspect of the invention, it is possible to evaluate the different chip patterns, i.e., the first chip patterns and the second chip patterns. Then, if there is no problem in the first chip patterns, only the first chip patterns can be exposed onto the wafer without wasting the exposure area of the projection exposure apparatus in the following step. As a result, the time for processing the wafer is shortened.

Further, if there is no problem in the first chip patterns, it is not necessary to redesign or re-fabricate a photomask when transferring from the first step to the second step, thereby shortening the developing time and reducing the fabricating cost of the photomask.

If there is any problem in the first chip patterns and there is no problem in the second chip patterns of the second mask pattern, the photomask where the second chip patterns are formed at the maximum exposure area of the projection exposure apparatus may be immediately designed and fabricated. Accordingly, the developing time of the chips is shortened compared with the case where the first mask pattern alone is formed on the photomask.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a perspective view showing a projection exposure apparatus

according to an embodiment of the invention;

Figs. 2 is a perspective view showing a multichip mask according to the embodiment of the invention;

Fig. 3 is a circuit diagram showing a chip pattern A formed on the multichip mask according to the embodiment of the invention;

Fig. 4 is a circuit diagram showing a chip pattern B formed on the multichip mask according to the embodiment of the invention;

Fig. 5 is a circuit diagram showing a chip pattern C formed on the multichip mask according to the embodiment of the invention;

Fig. 6 is a circuit diagram showing a chip pattern D formed on the multichip mask according to the embodiment of the invention;

Fig. 7 is a circuit diagram showing a chip pattern E formed on the multichip mask according to the embodiment of the invention;

Fig. 8 is a flowchart showing a fabricating flow of the chip A which is fabricated by use of the multichip mask according to the embodiment of the invention;

Fig. 9(A) is a view showing a multichip mask according to the embodiment of the invention and Fig. 9(B) is a view showing a wafer according to the embodiment of the invention;

Fig. 10(A) is a view showing a multichip mask according to the embodiment of the invention and Fig. 10(B) is a view showing a wafer according to the embodiment of the invention;

Fig. 11(A) is a view showing a multichip mask according to the embodiment of the invention and Fig. 11(B) is a view showing a wafer according to the embodiment of the invention;

Fig. 12(A) is a view showing a multichip mask according to the embodiment of the invention and Fig. 12(B) is a view showing a wafer according to the embodiment of the invention;

Fig. 13 is a flowchart showing a fabricating flow of the chip B which is fabricated by use of the multichip mask according to the embodiment of the invention;

Fig. 14(A) is a view showing the multichip mask according to the embodiment of the invention and Fig. 14(B) is a view showing a wafer according to the embodiment of the invention;

Fig. 15(A) is a view showing a conventional multichip mask and Fig. 15(B) is a view showing a conventional wafer; and

Fig. 16 is a perspective view showing a conventional projection exposure apparatus.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

A preferred embodiment of the present invention is now described with reference to the accompanying drawings.

As shown in Fig. 1, according to a projection exposure apparatus 10 (the apparatus is called as aligner or stepper.), a multichip mask 12 on which multiple types of chip patterns are formed longitudinally and horizontally is set on a reticle stage 14. A projection lens 16, and a wafer stage 18 are respectively disposed under the reticle stage 14. A wafer 20 is set on the wafer stage 18.

According to the aligner 10, light is allowed to enter a maximum

exposure area (as illustrated in net in Fig. 1) of the multichip mask 12 to expose each chip pattern. An exposed image of each chip pattern is reduced by the projection lens 16 and transferred onto the wafer 20.

At this time, the reticle stage 14 is moved in the direction of the arrows A and B in the same figure to change an incident area of light while the wafer stage 18 is moved in the direction of arrows C and D so as to transfer multiple types of chip patterns onto the wafer 20 at given positions.

As shown in Fig. 2, five types of chip patterns A, B, C, D, E are formed on the multichip mask 12. The chip patterns A number of which is nine in total are arranged vertically and horizontally by three at the center of the multichip mask 12. An area 22 (illustrated as half-tone dot meshing) serving as the main mask pattern on which nine chip patterns A are disposed forms a maximum exposure area of the projection exposure apparatus 10.

Three chip patterns B are arranged vertically in series on an area 24 which is a sub-mask pattern and provided at the periphery of the area 22 at the left side of the area 22, wherein three chip patterns C are arranged horizontally at the upper side of the area 22. Further, three chip patterns D are arranged vertically in series at the right side of the area 22 and three chip patterns E are arranged horizontally in series at the lower side of the area 22.

For example, if the area 24 is concentrically provided at one spot adjacent to the area 22, an area where chip patterns are arranged becomes long sideways, to form a wasteful area at the upper and lower portions of the mask. However, when the area 24 is provided in disperse at the periphery of the area 22, an area of the multichip mask 12 can be effectively utilized,

thereby not producing a useless area. Accordingly, a per-unit cost of the multichip mask 12 can be reduced.

All the chip patterns A, B, C, D and E are broad band operational amplifier circuits, and the constitutions thereof are described with reference to Fig. 3 to Fig. 7.

As shown in Fig. 3, the chip pattern A includes transistors Q_1, Q_2, ⋯, Q_{22}, resistors R_1, R_2, ⋯, R_{29}, capacitor C_1, and it amplifies an input data DIN from an external circuit, not shown, and outputs an output data RD.

Although the resistor R_{21} is included in the chip pattern A, and end of the resistor R_{21} is open. Accordingly, the resistor R_{21} does not substantially contribute to the circuit operation.

Next, as shown in Fig. 4, a chip pattern B includes transistors Q_1, Q_2, ⋯, Q_{22}, resistors R_1, R_2, ⋯, R_{29}, capacitors C_1, C_2 and is structured to add the capacitor C_2 to the chip pattern A (a portion encircled by the dotted line). The chip pattern B amplifies an input data DIN from an external circuit, not shown, and outputs an output data RD, in the same manner as the chip pattern A.

Next, as shown in Fig. 5, a chip pattern C includes transistors Q_1, Q_2, ⋯, Q_{22}, resistors R_1, R_2, ⋯, R_{29}, capacitors C_1, C_2 and C_3 and is structured to add the capacitor C_3 to the chip pattern B (a portion circled by the dotted line). The chip pattern C amplifies an input data DIN from an external circuit, not shown, and outputs an output data RD, in the same manner as the chip patterns A and B.

Next, as shown in Fig. 6, a chip pattern D includes transistors Q_1, Q_2, ⋯, Q_{22}, resistors R_1, R_2, ⋯, R_{29}, a capacitor C_1, and it is different from the

chip pattern A in respect of the constitution surrounded by the dotted line in the same figure. Since the both ends of the R_{21} are connected to other elements in the chip pattern D, the resistor R_{21} contributes to the circuit operation. However, the chip pattern D amplifies an input data DIN from an external circuit, not shown, and outputs an output data RD, in the same manner as the chip patterns A, B and C.

As shown in Fig. 7, a chip pattern E includes transistors Q_1, Q_2, ⋯, Q_{22}, resistors R_1, R_2, ⋯, R_{29}, capacitors C_1 and C_2 and is structured to add the capacitor C_2 to the chip pattern D (a portion encircled by the dotted line).

As set forth above, although the chip patterns A, B, C, D and E are different from one another in respect of the constitution of patterns in respect of the portions surrounded by the dotted lines in Fig. 3 to Fig. 7, they have the same function, and a chip pattern which is suitable for mass-production and exhibits an electric characteristic is selected among the chip patterns A, B, C, D and E.

A method of fabricating a chip is described next with reference to the flow chart in Fig. 8.

First, a program goes to step 200 where specification value of each chip to be mass-produced is set. Then, the program goes to step 202 where each chip to be mass-produced is presumed as a chip A corresponding to the chip pattern A. The chip A is evaluated and confirmed in electric characteristic before the program in the flow chart starts, and the electric characteristic at the time of evaluation satisfies the specification value which is set in step 200.

Then the program goes to step 204 where the devices of the chip

patterns B, C, D and E are designed. The chip patterns B, C, D and E having the same function as the chip pattern A and satisfying the specification value which is set in step 200 are designed by use of a computer and a designing software.

The program goes to step 206 where a mask data of the multichip mask 12, on which the chip pattern A and chip patterns B, C, D and E which are designed in step 204 are arranged as shown in Fig. 2, is prepared.

Next, the program goes to step 208 where the multichip mask 12 is fabricated. Mask data which is fabricated in step 206 is transferred to a data controller (not shown) of a mask drawing unit. A mask blank with resist (not shown) is set on the mask drawing unit, and pattern drawing data is exposed and drawn onto the resist of the mask blank with resist. Thereafter, a pattern is formed after a pattern developing step and the like, then the fabrication of the multichip mask 12 is completed after a pattern inspection step, a pattern correction step, and the like.

Subsequently, the program goes to step 210 where the wafer 20 is subjected to a processing. First, the multichip mask 12 is moved in the direction of the arrows A and B as shown in Fig. 1 so that an area 26 (depicted by the bold line in the same figure) including three chip patterns B of the multichip mask 12 shown in Fig. 9(A) at the left end and six chip patterns A at the right side of the chip patterns B is aligned with the maximum exposure area of the projection exposure apparatus 10.

Then, as shown in Fig. 1, the wafer stage 18 is moved in the direction of the arrows C and D so that the exposure area of the projection exposure apparatus 10 is aligned with a wafer area 28 at the upper left

portion of the wafer 20 shown in Fig. 9(B). Then, when the area 26 is subjected to exposure, exposed images of the chip patterns A and B are transferred to the wafer area 28.

Then, as shown in Fig. 10(A), an area 30 including three chip patterns C of the multichip mask 12 at the upper end and six chip patterns A at the lower side is shifted to a wafer area 32 adjacent to the right side of the wafer area 28 shown in Fig 10(B), namely, a transfer area of the wafer 20 is shifted counterclockwise to effect exposure.

Likewise, an area 34 including the chip patterns D and A shown in Fig. 11(A) is exposed to a wafer area 36 which is shifted counterclockwise from the wafer area 32 shown in Fig. 11(B), while an area 38 including the chip patterns E and A shown in Fig. 12(A) is exposed to a wafer area 40 which is shifted counterclockwise from the wafer area 36 shown in Fig. 12(B).

When the exposure of the chip patterns A, B, C, D and E is completed and the inspection of the wafer 20 is completed, the program goes to step 212 where prototypes of chips are assembled and subjected to a sealing or bonding treatment. Also in step 212, the prototypes of chips A, B, C, D and E corresponding to the chip patterns A, B, C, D and E are completed after a back grinding step, a dicing step and the like.

As shown in Fig. 12(B), a large number of chips A are fabricated compared with other chips. As a result, the time for fabricating the prototypes of chips A can be shortened, thereby ensuring the time of supply of the prototypes of chips A.

Subsequently, the program goes to step 214 where the prototypes of

chips A, B, C, D and E are evaluated and determined. If the chip A satisfies the specification value of the chip to be mass-produced which is set in step 200, it is determined that the chips A are mass-produced, then the program goes to step 216 where the chips A are mass-produced.

As shown in Fig. 2, the area 22 where the chip patterns A of the multichip mask 12 are formed at the time of prototyping the chips has the same size as the maximum exposure area of the projection exposure apparatus 10. Accordingly, the multichip mask 12 can be used as it is in the mass-production stage, and when the area 22 is subjected to exposure, the chip patterns A can be transferred onto the wafer 20 without wasting the exposure area of the projection exposure apparatus 10.

Further, it is not necessary to redesign and re-fabricate a reticle mask for mass-production, it is possible to transfer from a prototyping stage to a mass-production stage in a short period of time. Still further, a re-fabricating cost of the reticle mask can be reduced.

If the determination in step 214 where the determination of the chip pattern A is OK (affirmative), evaluation data of the chips B, C, D and E are recorded in step 218 in addition to the mass-production of the chips A. These data is of great utility in the next development stage.

Whereupon, if the determination is NG (negative) in step 214, a chip to be mass-produced is narrowed from the evaluated chips B, C, D and E in place of the chip A. A chip among the chips B, C, D and E, which satisfies the specification value in electric characteristic and suitable for mass-production, is assumed as a chip B.

As shown in a flow chart showing the fabrication of the chip in Fig.

13, the program goes to step 222 where a reticle mask 50 of the chip B shown in Fig. 14 is designed. In step 222, only the chip pattern B corresponding to the chip B is formed on the maximum exposure area of the projection exposure apparatus 10. In step 224, the reticle mask 50 is fabricated, and the program goes to step 226 where the wafer is subjected to processes. In step 222, only the chip pattern B is exposed onto a wafer 52.

Then the program goes to step 228 where the wafer is assembled and bonded so as to fabricate the prototype of the chip B, thereafter goes to step 230 where the chip B is evaluated and determined. If the electric characteristic of the chip B satisfies the chips for mass-production, the mass-production of the chip B is determined, and goes to step 232 where the chips B are mass-produced.

Although the flow chart showing the fabrication of the chip B was described, the chips B, C, D and E have to be evaluated immediately after the determination of NG of the chip A in place of the chip A. This is caused by the fact that the chip patterns B, C, D and E are formed on the multichip mask 12 which was used when prototyping the chip A. As a result, the time taken from the determination of NG of the chip A to the mass-production of the chip B is shortened.

According to the preferred embodiment of the invention, all the chip patterns B, C, D and E have the same function as the chip pattern A, and a chip pattern corresponding to a chip to be mass-produced is selected from five types of chip patterns, but the invention is not limited to such examples, and hence any of the chip patterns B, C, D and E may have a chip pattern having the function completely different from that of the chip pattern A.

In this case, a new circuit to be evaluated is formed on the same multichip mask and subjected to prototyping and evaluation so that the time for developing the next stage chip can be shortened. Further, with the evaluation set forth above, it is conjectured as a chip pattern corresponding to a chip to be mass-produced like the chip pattern A as illustrated in a preferred embodiment of the invention.

With the construction of the invention, the chips can be prototyped and mass-produced by the same photomask, and the exposing area of the projection exposure apparatus can be utilized to the greatest extent.